REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on April 3, 2003, and the references cited therewith.

Claims 1-3, 16, 18-24, 26, 28, 30-33 and 41 are amended, and claims 4-15, 25, 27, 29, 34-40 are canceled; as a result, claims 1-3, 16-24, 26, 28, 20-33 and 41 are now pending in this application.

Double Patenting Rejection

Claims 1, 2 and 18-41 of this application conflict with claims 1-21 of Application No. 09/637,532. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application. Applicant is required to either cancel the conflict claims from all but one application or maintain a clear line of demarcation between the applications.

Claims 1, 2, 18 to 24, 26, 28, 30-33 and 41 in this application have been amended to claim subject matter distinct from subject matter claimed in Application No. 09/637,532. Claims 25, 27, 29 and 34-40 have been cancelled. Applicant respectfully submits that there are no conflicting claims and hence no double patenting.

§102 Rejection of the Claims

Claims 1, 2, 18-22, 26, 27, 30 and 33-35 were rejected under 35 USC § 102(b) as being anticipated by both Vassiliadis (U.S. Patent No. 5,187,679) and Niehaus (U.S. Patent No. 4,399,517).

Claims 1, 2, 18, 19 and 20 as amended now define that the logic circuit is divided into a plurality of EXOR logic units. Each EXOR logic unit generates outputs as elementary EXOR symmetric functions of the inputs. In Vassiliadis there is no such arrangement. The only use of EXOR logic is in the generation of the first binary output S. This does not include the use of sub logic units as claimed in amended claim 1. Vassiliadis has not realised the possibility of being able to break down the EXOR symmetric function into smaller EXOR symmetric functions. In

Niehaus there is no disclosure of the use of elementary EXOR symmetric functions for the generation of the binary outputs.

Claims 21, 22, 26, 30 and 33 as amended now define that the logic circuit generates at least two of the plurality of binary outputs as elementary EXOR symmetric functions of the binary inputs. Vassiliadis only discloses a circuit in which only the least significant binary output is generated as an elementary EXOR symmetric function. Vasiliadis has failed to identify the possibility of generating other of the binary outputs as elementary EXOR symmetric functions. In Niehaus there is no disclosure of the use of elementary EXOR symmetric functions for the generation of the binary outputs.

With regards to Claims 27, 34 and 35, these claims have been cancelled and thus the examiners objections are moot.

It is therefore respectfully submitted that the subject matter of claims 1, 2, 18-22, 30 and 33 are not anticipated by both Vassiliadis and Niehaus. Applicant respectfully requests that the rejection under 35 USC § 102 be withdrawn.

Claim 36 was rejected under 35 USC § 102(b) as being anticipated by Chiu (U.S. Patent No. 5,325,320).

With regard to claim 36, this claim has been cancelled and thus the examiners objection is moot.

§112 Rejection of the Claims

Claims 1-41 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which application regards as the invention.

Claim 1 has been amended to more particularly point out the claimed invention and a clear definition of the phrase symmetric function has been included. Amended claim 1 is clearly illustrated in the embodiment of figures 19 to 21. The EXOR logic units in this embodiment comprise the logic blocks 5 and 6.

With regard to claim 2 and claim 3, applicant respectfully submits that these claims are clearly illustrated in the embodiment of figures 15 to 18.

With regard to claims 4 to 15, 25, 27, 29 and 34 to 40, these claims are now cancelled and thus the objections of the examiner are moot.

With regard to claim 16, this claim has been amended to be an independent claim.

With regard to claim 17, although the Office Action states: "Claims 1-41 are rejected under 35 USC 112 ," the body of the Office Action does not provide any specific reasons as to why claim 17 is rejected. Thus, the Office Action fails to meet the requirements of at least:
1. 37 CFR § 1.104(a)(2): "The reasons for any adverse action or any objection or requirement will be stated in an Office action and such information or references will be given as may be useful in aiding the applicant."

Claims 18 to 20 have been amended to be independent claims consistent with amended claim 1. Claim 18 is described in detail on page 22 line 16 to page 23 line 3. Claim 19 is described on page 23 lines 4 to 9. Claim 20 is described in detail on page 23 lines 9 and 10.

With regard to claims 23 and 24, applicant respectfully submits that these claims are described in detail in the embodiment illustrated in figures 19 to 21.

With regard to claim 28, applicant respectfully submits that this claim is described in detail in the embodiment illustrated in figures 15 to 18.

Therefore, Applicant respectfully requests that the rejection of claims 1-41 under 35 USC § 112 be withdrawn.

Documents Cited but Not Relied upon for this Office Action

Applicant need not respond to the assertion of pertinence stated for the references cited but not relied upon by the Office Action since these references are not made part of the rejections in this Office Action. Applicant is expressly not admitting to this assertion and reserves the right to address the assertion should it form part of future rejections.

Claim Objections

Claim 41 was objected to under 37 CFR 1.75 as being in improper form because a multiple dependent claim should refer to other claims in the alternate only.

Claim 41 has been amended to be in proper form and to refer to multiple claims only in the alternative. Withdrawal of the objection to Claim 41 is respectfully submitted.

Priority

Applicant filed a Communication Regarding Filing of Priority Document in Accordance with 35 USC 119 and a Certified Copy of Great Britain Application No. 0019287.2 on December 19, 2001 and which was received by the Office of Initial Patent Examination of January 18, 2002 which is evidenced by a copy of the stamped postcard. Please inform us if you would like us to file an additional certified copy.

Drawings

Applicant respectfully submits that Figure 26 is referred to in the description on page 25 at line 12.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 349-9592) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 3rd day of October, 2003.

PATRICIA A. HULTMAN

Name Signature